Opamp integrators

1 Simple op-amp integrator

Consider the basic opamp integrator circuit in Figure 1. We know that, in the time-domain, the output voltage is

$$v_o = -\frac{1}{RC}\int v_i dt \tag{1}$$

For example, if the input is a constant DC voltage of magnitude A, the output will be of the form

$$v_o(t) = -\frac{1}{RC}\int A dt = -\frac{A}{RC}\int dt = -\frac{A}{RC}t. \tag{2}$$

It is also useful to consider the behaviour in the frequency domain however.

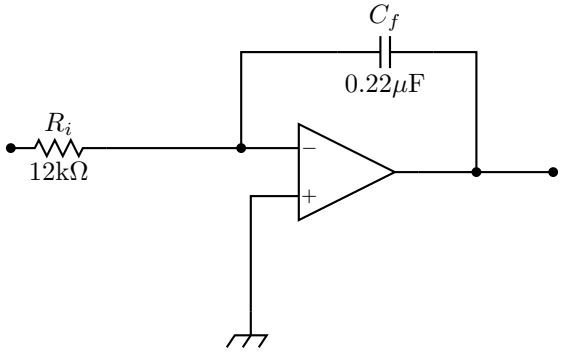

Figure 1: Simple integrator

1.1 Closed-loop response

An important observation is that the output voltage, V_o, is the open-loop gain times the input voltage, V.

$$\begin{aligned} V_o &= -A_{OL_{mid}}(V_- - V_+) = -A_{OL_{mid}}V \\ V &= -\frac{V_o}{A_{OL_{mid}}} \end{aligned} \tag{3}$$

In the frequency domain,

$$i_i = i_f$$

$$\frac{V_i - V}{R_i} = -\frac{V_o - V}{Z_{C_f}} = -\frac{V_o - V}{\frac{1}{j2\pi f C_f}}$$

$$\frac{V_i - V}{R_i} = -j2\pi f C_f (V_o - V)$$

$$V_i + \frac{V_o}{A_{OL_{mid}}} = -j2\pi f R_i C_f \left(V_o + \frac{V_o}{A_{OL_{mid}}} \right)$$

$$V_i = -V_o \left(\frac{j2\pi f R_i C_f}{A_{OL_{mid}}} + j2\pi f R_i C_f + \frac{1}{A_{OL_{mid}}} \right)$$

$$V_i = -V_o \left(\frac{j2\pi f R_i C_f + A_{OL_{mid}} j2\pi f R_i C_f + 1}{A_{OL_{mid}}} \right)$$

$$\frac{V_o}{V_i} = -\frac{A_{OL_{mid}}}{j2\pi f R_i C_f (1 + A_{OL_{mid}}) + 1}$$

So

$$\frac{V_o}{V_i} = -\frac{A_{OL_{mid}}}{1 + jf/f_0}$$

where

$$f_0 = \frac{1}{2\pi R_i C_f (1 + A_{OL_{mid}})}.$$

Considering only the magnitude, we have

$$\boxed{A_{CL}(f) = -\frac{A_{OL_{mid}}}{1 + jf/f_0}}. \tag{4}$$

1.2 Pspice simulation

Note that, for $f \ll f_0$,

$$|A_{CL}(f)| \to A_{OL_{mid}}.$$

Thus, DC and very low-frequency signals are amplified at maximum gain. The input offset voltage V_{io} and bias currents i_{b_-} and i_{b_+} are three such low-frequency signals. Thus, they are amplified at maximum gain, and drive the op-amp into saturation (Figure 3).

Integrator response to a constant voltage — a ramp The input offset voltage is low-frequency, and we can regard it as a DC signal for the present purposes. Then, from equation 2, we know that the output is

$$v_o(t) = -\frac{1}{RC} \int v_{io} dt = -\frac{A}{12\text{k}\Omega \cdot .22\mu\text{F}} t,$$

where v_{io} is the input offset voltage, and A is its magnitude. I.e., the response of an integrator to a constant input is a *ramp*. In this case, however, the output is limited by the maximum value of the op-amp power supply — approx. 15 V (Figure 3).

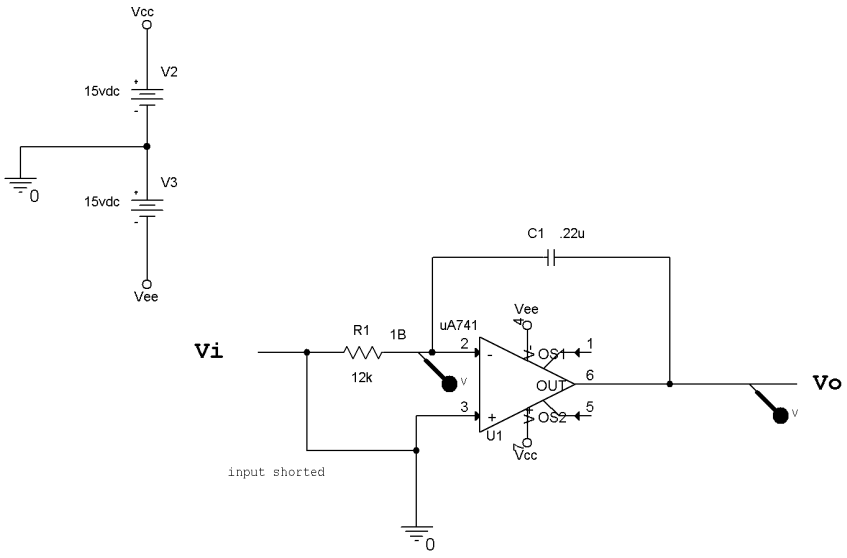

Figure 2: Simple integrator with input shorted. The output voltage can be due only to an offset bias in the input.

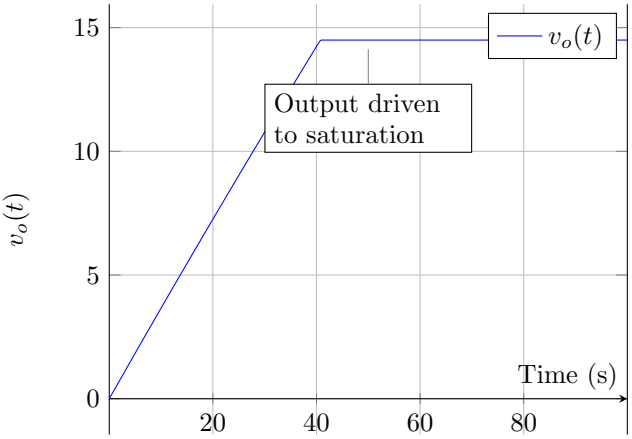

Figure 3: Simple integrator — Pspice output

Magnitude of the input offset voltage, v_{io} From inspection of the Pspice results in Figure 3, we see that $v(t = 20\text{s}) = 7.5\text{V}$. Thus,

$$-\frac{A}{12\text{k}\Omega \cdot .22\mu\text{F}}(20\text{s}) = 7.5\text{V}$$

$$\implies A = \frac{7.5\text{V}(12\text{k}\Omega)(.22\mu\text{F})}{20\text{s}} \approx -.99\text{mV}.$$

$$\boxed{v_{io} = A = -.99\text{mV}}$$

2 Practical integrator with limited DC feedback

To mitigate the problem of output saturation due to non-zero input offset voltage, we introduce a resistor R_f in parallel with C_f to limit the feedback for DC and very low frequency input signals. Having done this, the frequency response becomes

$$A_{CL}(f) = -\frac{A_{CL_{mid}}}{1 + jf/f_0}, \tag{5}$$

where $A_{CL_{mid}} = R_f/R_i$, and $f_0 = \frac{1}{2\pi R_f C_f}$.

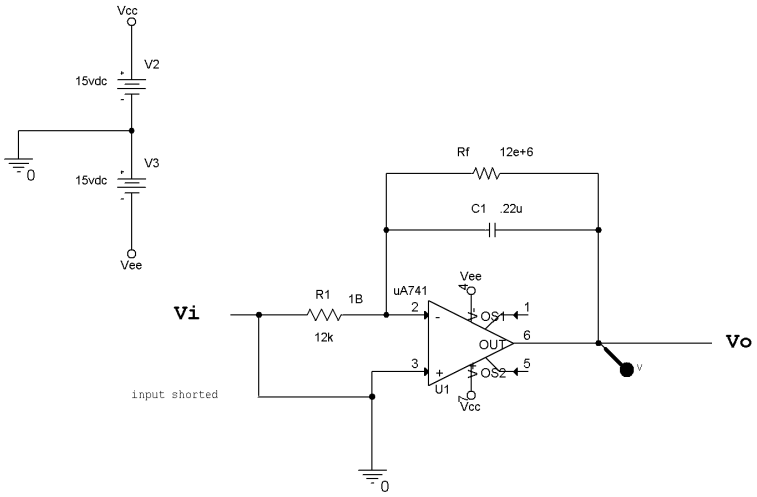

Figure 4: Limiting the DC feedback using R_f

This is actually a first-order system — or low-pass filter. Thus, we expect the time-domain output to be of the form

$$v_o(t) = A \cdot A_{CL_{mid}} \left(1 - e^{-\frac{t}{\tau}}\right), \tag{6}$$

where $\tau = R_f C_f$ is the time-constant, $A_{CL_{mid}} = R_f/R_i$ is the filter gain, and A is the amplitude of the input.

With the values of R_i, C_f and R_f indicated, we expect the gain and phase responses shown in Figure 5. The time-constant is

$$\tau = R_f C_f = 12 \times 10^6 \times .22 \times 10^{-6} = 2.64\text{s}.$$

Thus, we expect the output to stablize after $5\tau \approx 13$ seconds. The breakpoint frequency is

$$w_0 = \frac{1}{\tau} = .379\text{rad/s},$$

or, in Hertz,

$$f_0 = \frac{1}{2\pi\tau} \approx 60.3\text{mHz}.$$

The magnitude of the input offset voltage, A, is as determined previously:

$$v_{io} = A = -0.99\text{mV}.$$

Upon simulating this configuration in Pspice (Figure 4), we got the results

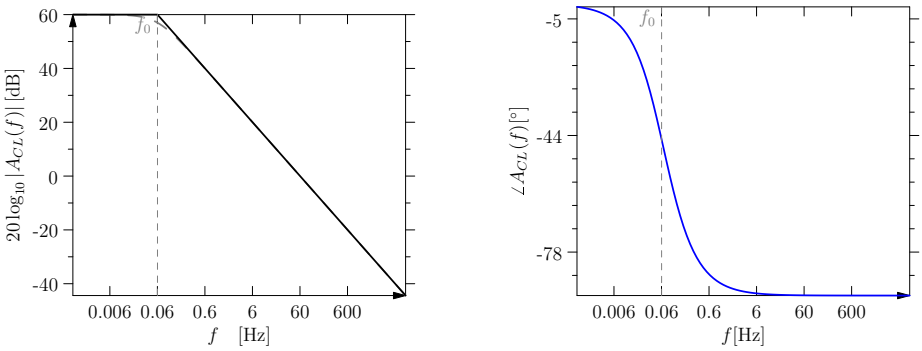

Figure 5: Gain and phase response of practical integrator

shown in Figure 6.

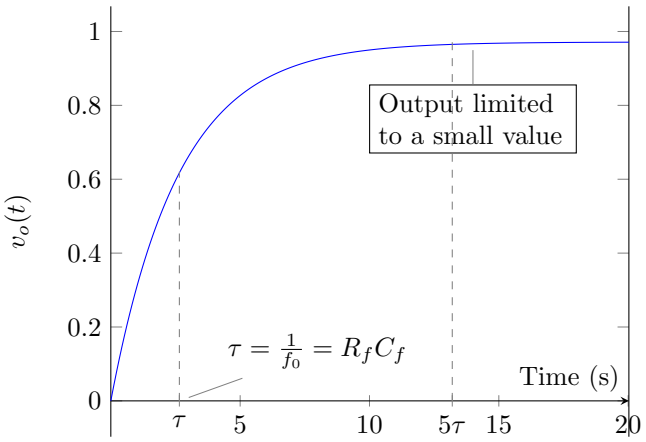

Figure 6: Pspice results

3 Sinusoidal input

When we input a sinusoidal input to the circuit, the output is 90 degrees out of phase as expected (Figure 7). Note that the magnitude of the output is approximately equal to that of the input. The frequency of the input $f = 60\text{Hz}$ is three decades above the breakpoint frequency. Since the closed-loop mid-band gain is 60 dB, and since $A_{CL}(f)$ falls at a rate of 20 dB per decade after the breakpoint frequency, we must have

$$A_{CL}(60\text{Hz}) = 0\text{dB}$$

. This can be observed in Figure 10.

3.1 Phase response

Note that we are using a 60 Hz sinusoidal input. This frequency is three decades above ehe breakpoint frequency, f_0. We note from Figure 5 that the phase of the frequency response declines at a rate of 45° per decade on either side of f_0 and is essentially level otherwise.

We expect the phase response at this frequency to be

$$\angle A_{CL}(60) = \angle \left(\frac{-A_{CL_{mid}}}{1 + \frac{j60}{60.3\text{mHz}}} \right) \approx 90°.$$

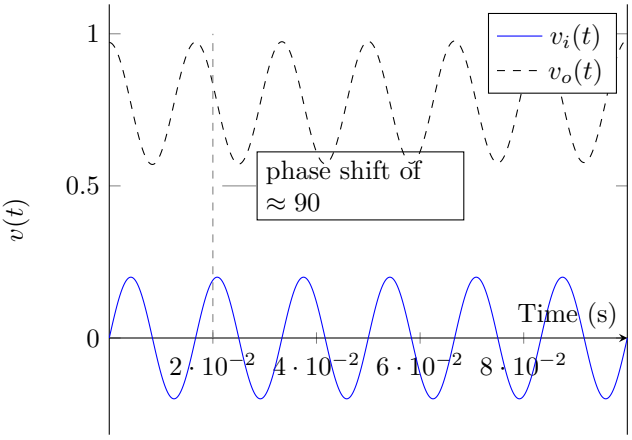

Figure 7: Integrator response to a sinusoidal input

4 Square-wave input

When we input a square wave, we expect a triangle wave output.

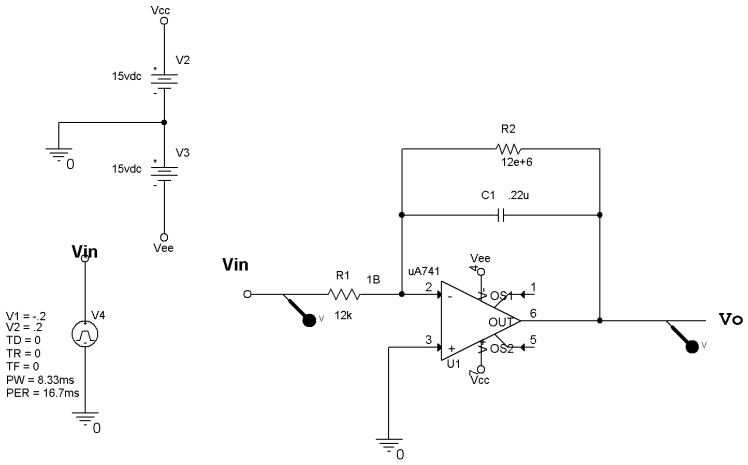

Figure 8: Square-wave input

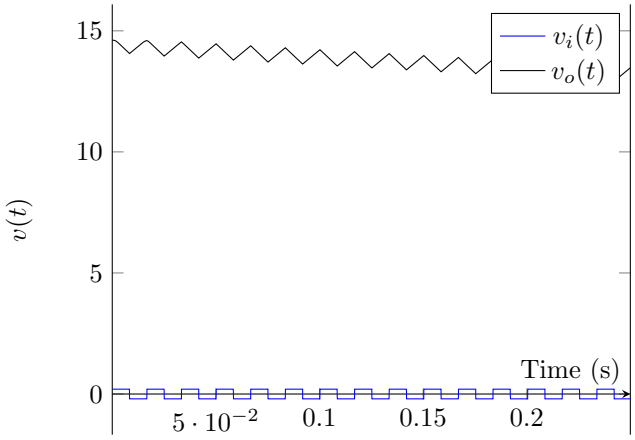

Figure 9: Integrator response to a square-wave input

5 AC sweep

Closed-loop gain fall-off From Figure 10, we see that the fall-off rate for $A_{CL}(f)$ is 20 dB per decade.

DC closed-loop gain The closed-loop DC gain is 60dB = 1000.

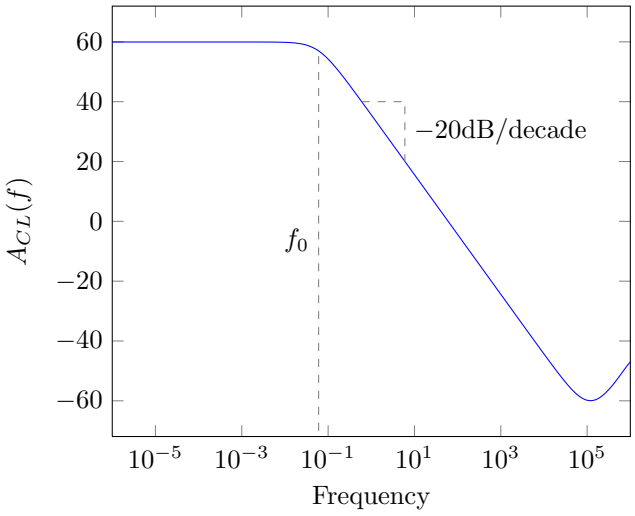

Figure 10: Frequency response of circuit